REMARKS

This application has been reviewed in light of the Office Action dated April 30, 2003. Claims 31, 33-51, 55, 57-62, and 65-71 are pending in this application. Claims 32 and 56 have been cancelled, without prejudice or disclaimer of subject matter. Applicants note that the recitation of Claim 32 was incorporated into Claims 31 and 47, and the recitation of Claim 56 was incorporated into Claims 51 and 55. Claims 70 and 71 have been added to provide Applicants with a more complete scope of protection. Claims 31, 47, 51, and 55, which are the independent claims, have been amended to define still more clearly what Applicants regard as their invention, in terms that distinguish over the art of record. Claims 33, 34, 36-38, 41-43, 48-50, 57-62, and 65-69 have been amended as to matters of form only and those amendments do not, in any way, narrow the scope of any of those claims. Favorable reconsideration is requested.

The Office Action rejected Claims 31, 47, 51, and 55 under 35 U.S.C. § 112, second paragraph, as both indefinite and incomplete, asserting that "there is no structural relationship to [a] memory element on the printhead substrate as to the data recording and write means, and the write inhibition means recited in these claims." Applicants have amended these claims to delete the recitation "a memory unit mounted on said print head substrate" and consequently, this rejection is moot.

The Office Action rejected Claims 31-36, 39-43, 45-51, 55-63, and 65-69 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,610,635 A (Murray et al.) in view of U.S. Patent No. 6,318,850 B1 (Childers et al.); Claims 37, 44, and 63 as being unpatentable over Murray et al. in view of Childers et al., and further in view of U.S. Patent No. 6,168,251 B1 (Imanaka et al.); and Claims 38, 46, and 64 as being unpatentable over Murray et al. in view of Childers et al., and further in view of National Semiconductor, Corp., 1981 Logic Databook, 1981, pp. 6-98-101. Cancellation of Claims

32, 56, 63, and 64 renders their rejections moot. Applicants respectfully traverse these rejections.

Initially, Applicants submit that U.S. Patent No. 6,610,635 A (Murray et al.) was not correctly cited in the Office Action, thus Applicants cannot respond to the assertions made in the Office Action by the Examiner regarding Murray et al., and no prima facie case of obviousness has been made out. This patent was not cited by Applicants in any Information Disclosure Statement submitted to the Office in this case, nor in any Notice of References included with any of the Office Actions issued in this case, and was not discussed or noted in the parent of this application.[1]

Applicants submit that amended independent Claims 31, 47, 51, and 55, together with the remaining claims dependent thereon, are patentably distinct from Childers et al. at least for the following reasons, even assuming the existence of a reference showing all that "Murray et al." was cited for.

The aspect of the present invention set forth in Claim 31 is a head substrate of a printing head capable of being detachably mounted on a printer main body. The head substrate includes plural external connection terminals for externally entering various signals and electric power, and recording means for recording according to the various signals. A data memory means of the head substrate executes data writing and data readout, and a memory access means executes the data writing into the data memory means in response to the various signals and the electric power and the data readout corresponding to the various signals. The writing inhibition means of the head substrate permanently disables the data writing into the data memory means by the memory access means, and the

---

1/ A search on the U.S. Patent and Trademark Office's website revealed that U.S. Patent No. 6,610,635 issued to P. Khatri on August 26, 2003; relating to a dry thermal interface material (the first page of which is attached hereto).

writing inhibition means is adapted for cutting off electric power wiring for supplying the electric power for data writing from the external connection terminals to the memory access means.

One important feature of Claim 31 is the writing inhibition means that permanently disables the data writing to the data memory means by cutting off electric power wiring used to supply the electric power to the data wiring. With this feature, and the combination of the other features of Claim 31, even when noises or signals caused as a result of a malfunction are applied at the replacement of the recording head, it is not possible that data stored is rewritten improperly.

Childers et al., as understood by Applicants, relates to an ink container refurbishment system. The Office Action states that Childers et al. discloses "a memory device that has write enable protection and permanent disabling of the write enable line by electronic means" and asserts that column 7, lines 23-25, and lines 33-37, and Figure 5, reference numeral 34, provides support for this assertion. Applicants note that column 7, lines 23-25 state that a "[m]emory device 34 has a protected section, a write-once section, and a multiple write/erase section" and lines 33-37 state that "[t]he printing system control electronics then records a parameter onto the protected portion of memory device 34 that is indicative of the initial receiving coil voltage. The printing system control electronics then initiates a write protect feature to assure that the information in the protected portion of memory is not altered." Applicants also note that reference numeral 34 of Figure 5 depicts an information storage (memory) device of an ink container. Applicants submit that Childers et al. discusses a memory device 34, and a write protect feature that apparently assures that information in the protected portion of the memory is not altered. However, Applicants have not found anything in this section, or any other section of Childers et al., that would teach or suggest a writing inhibition means for permanently disabling the data

writing to a data memory means by cutting off electric power wiring to the data wiring.

Accordingly, at least for this reason, Applicants submit that Claim 31 is patentable over "Murray et al." and Childers et al.

Independent Claims 47, 51, and 55 include the same features of a writing inhibition means for permanently disabling the data writing to a data memory means, and for cutting off electric power wiring to the data wiring, as discussed above in connection with Claim 31. Accordingly, Claims 47, 51, and 55 are believed to be patentable for at least the same reasons as discussed above in connection with Claim 31.

A review of the other art of record, including Imanaka et al. and National Semiconductor, Corp., 1981 Logic Databook, has failed to reveal anything that, in Applicants' opinion, would remedy the deficiencies of the art discussed above, as applied against the independent claims herein. Therefore, those claims are respectfully submitted to be patentable over the art of record.

The other claims in this application, including new claims 70 and 71, depend from one or another of the independent claims discussed above, and, therefore, are submitted to be patentable for at least the same reasons. Since each dependent claim is also deemed to define an additional aspect of the invention, individual consideration or reconsideration, as the case may be, of the patentability of each claim on its own merits is respectfully requested.

In view of the foregoing amendments and remarks, Applicants respectfully request favorable reconsideration and early passage to issue of the present application.

Applicants' undersigned attorney may be reached in our New York Office by telephone at (212) 218-2100. All correspondence should continue to be directed to our address listed below.

Respectfully submitted,

Peter G. Thurlow

Attorney for Applicants

Registration No. 47,138

FITZPATRICK, CELLA, HARPER & SCINTO
30 Rockefeller Plaza
New York, New York 10112-3801
Facsimile: (212) 218-2200

NY_MAIN 372761v1

United States Patent ***6,610,635***
Khatri **August 26, 2003**

Dry thermal interface material

Abstract

A thermal interface material including a compound which has high thermal conductivity, is dry-to-the-touch, but naturally tacky, and may be formed into various shapes, such as sheets and blocks, to serve as a heat transfer material for electronic components. The compound includes a pre-blend of a polyol ester and an antioxidant, a filler(s), a high viscosity oil, and either a solvent, a surfactant, and a polystyrene-based polymer, or aluminum silicate. A method for using the compound includes the steps of providing a heat generating electronic component with a first surface; providing a heat dissipating component with a second surface with which the first surface is to interface; and disposing the compound between the respective surfaces to effectuate efficient heat transfer therebetween. Further, the compound can be applied alone, e.g., layered, sprayed, or screen printed, can be applied to a thermally conductive foil backing, or a thermally conductive and electrically insulative backing, or formed into shapes such as blocks or sheets. Also, removable liners can be applied to exposed surfaces of the compound to facilitate handling, shipping and storage, but are removed prior to the compound being applied between the electronic component and the heat sink.

Inventors: **Khatri; Prakash** (Matawan, NJ)
Assignee: **AOS Thermal Compounds** (Eatontown, NJ)
Appl. No.: **951501**
Filed: **September 14, 2001**

Current U.S. Class: **508/161**; 508/172; 508/178; 508/485; 508/591; 361/704
Intern'l Class: C10M 113/08; C10M 169/02; H05K 007/20
Field of Search: 508/172,178,161

References Cited [Referenced By]

U.S. Patent Documents

3669884	Jun., 1972	Wright	252/36.